

**PATENT**

**IN THE UNITED STATES PATENT OFFICE**

In re application of:

Sam Yang

Serial No.: Not Assigned

Filed: Concurrently Herewith (September 8, 2003)

For: **METHOD FOR FORMING A RUTHENIUM  
METAL LAYER**

§

§ Group Art Unit: Not Assigned

§

§ Examiner: Not Assigned

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§ Atty. Docket: 2000-0719.01/US

§

§ Paper No. \*

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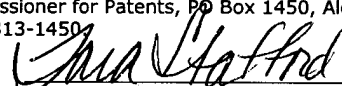
Mail Stop Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate of Express Mailing (37 CFR §1.10)**

"Express Mail" mail number: ET658404597US

Date of Deposit: September 8, 2003

I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

  
Signature

Dear Sir:

**INFORMATION DISCLOSURE STATEMENT**

In compliance with the duty of disclosure under 37 CFR §1.56, Applicant respectfully requests entry of this Information Disclosure Statement, and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. As the references consist only of patent documents cumulative from the parent, copies are not enclosed.

In accordance with 37 CFR §1.97(b), this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 CFR §1.56(a) exists.

The following reference is submitted for the Examiner's review:

**U.S. Patent Documents**

Document No.	Date	Inventor
5,852,307	12/1998	Aoyama et al.
6,037,206	03/2000	Huang et al.
6,278,152	08/2001	Hieda et al.
6,284,587	09/2001	Yamauchi et al.
6,475,854	11/2002	Narwankar et al.
US 2002/0037630	03/2002	Agarwal et al.

**Other References:**

"In-situ Barrier Formation for High Reliable W/Barrier/poly-Si Gate Using Denudation of WNX on Polycrystalline Si", Byung Hak Lee et al., R & D Division, LG Semicon Co. Ltd., 1 Hyangjeong-dong, Cheongju-si, 361-480, Korea, 9/98.

"Tungsten Gate Structure Formed by Reduced Temperature Conversion of Tungsten Nitride", C.J. Galewski et al., Genus Inc.

Copending Application: "Method for Forming and Integrated Circuit Structures Containing Ruthenium and Tungsten Containing Layers", Serial Number 09/590,795, Docket Number 6047-53173, Filed June 8, 2000.

As this Information Disclosure Statement is being submitted before the mailing of a first Office Action on the merits, no fee is due. However, the Commissioner is authorized to charge any required fee to Micron Technology Inc. Deposit Account No.13-3092, Order No. 2000-0719.01/US.

If there are any matters which may be resolved or clarified through telephone interview, the Examiner is respectfully requested to contact Applicant's undersigned agent at the number indicated.

\* \* \* \*

A Form PTO-1449 is enclosed herewith.

Respectfully submitted,



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FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: <b>2000-0719.01/US</b>	Serial No: <b>Not Assigned</b>
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		Applicant: <b>Micron Technology, Inc.</b>	
(37 CFR 1.98(b))                      (use several sheets if necessary)		Filing Date: <b>September 8, 2003</b>	Group: <b>Not Assigned</b>

**U.S. PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Name	Class	Subclass	
AA	5,852,307	12/1998	Aoyama et al.	257	295	
AB	6,037,206	03/2000	Huang et al.	438	240	
AC	6,278,152	08/2001	Hieda et al.	257	306	
AD	6,284,587	09/2001	Yamauchi et al.	438	240	
AE	6,475,854	11/2002	Narwankar et al.	438	238	
AF	US 2002/0037630	03/2002	Agarwal et al.	438	430	
AG						
AH						
AI						
AJ						
AK						

**FOREIGN PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
AL						<input type="checkbox"/>	<input type="checkbox"/>
AM						<input type="checkbox"/>	<input type="checkbox"/>
AN						<input type="checkbox"/>	<input type="checkbox"/>

Initial		<b>OTHER ART</b> (including author, title, date, pertinent pages, etc.)
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	AO		"In-situ Barrier Formation for High Reliable W/Barrier/poly-Si Gate Using Denudation of WNX on Polycrystalline Si", Byung Hak Lee et al., R & D Division, LG Semicon Co. Ltd., 1 Hyangjeong-dong, Cheongju-si, 361-480, Korea, 9/98.
	AP		"Tungsten Gate Structure Formed by Reduced Temperature Conversion of Tungsten Nitride", C.J. Galewski et al., Genus Inc.
	AQ		Copending Application: "Method for Forming and Integrated Circuit Structures Containing Ruthenium and Tungsten Containing Layers", Serial Number 09/590,795, Docket Number 6047-53173, Filed June 8, 2000.
	AR		

Examiner:	Date Considered:
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (37 CFR 1.98(b)) <span style="margin-left: 50px;">(use several sheets if necessary)</span>		Applicant: <b>Micron Technology, Inc.</b>	
		Filing Date: <b>September 8, 2003</b>	Group: <b>Not Assigned</b>

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